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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/937,877	09/29/1997	ANATOLIY V. TSYRGANOVICH	ZILG-183US0	2256

7590 10/22/2002

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EXAMINER
SRIVASTAVA, VIVEK

ART UNIT	PAPER NUMBER
2611	13

DATE MAILED: 10/22/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

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This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

OFFICE ACTION SUMMARY

☒ Responsive to communication(s) filed on 2/21/02.

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 D.C. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) 4, 5, 7, 10, 12-31 + 32-35 is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☒ Claim(s) 4, 5, 7, 10, 20-24, 26 and 29-35 is/are allowed.

☒ Claim(s) 13, 14-19, 25, 27, 28 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☐ Notice of Reference Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

-- SEE OFFICE ACTION ON THE FOLLOWING PAGES --

* U.S. GPO: 1996-409-290/40029

DETAILED ACTION

Claim Rejections - 35 U.S.C. § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 13, 14 - 19, 25, 27 and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Kobayashi et al.

Considering claim 13, Kobayashi discloses the claimed providing a circuit, inputting an input signal into the circuit such that the circuit filters the input signal to provide a filtered component to the output of the circuit (fig 5 items 21 and 22), inputting an adjustment signal into the circuit so that the adjustment signal provides an unfiltered offset that is added to the output (fig 5 adjustments coefficients K2 and K1 will change the level of output Dvec, the signal K2 x Do(N+1 is added to the delayed or filtered signal K1 x DoN), adding the adjustment signal to the input signal (figure 5, the signal K2 x Do(N+1 is added to the delayed or filtered signal K1 x DoN).

Considering claim 14, Kobayashi inherently discloses wherein the adjustment signal keeps the output within a preset range (col 4 lines 23 - 68, adjustment signal must keep output in a preset range in order to maintain a correct output).

Considering claims 15 and 19, Kobayashi discloses filtering of the input signal is a low-pass filtering (see frequency response in fig 6C from time t0 - t).

Considering claim 16, Kobayashi discloses the claimed wherein the input is a phase signal (col 4 lines 24 - 59).

Considering claims 17 and 27, Kobayashi discloses wherein the input is a hue signal (col 1 lines 7 - 11).

Considering claims 18 and 28, Kobayashi inherently discloses constraining a phase signal within a finite preset range (Kobayashi discloses correcting or adjusting the input phase, thus output phase is inherently constrained within a preset range in order to have an adjusted correct output) , the constraining step including adding a correction signal to the phase signal (fig 5), filtering the phase signal without filtering the correction signal portion of the phase signal (fig 5, when no adjusting is required, resulting in K2 and K1 equal to one, the circuits acts like a filter), and adding the correction signal to the phase signal (figure 5, the signal K2 x Do(N+1) is added to the delayed or filtered signal K1 x DoN).

Considering claim 25, Kobayashi discloses wherein the constraining step is such that the phase signal is processed so as to use a differential input (see fig 5, differential phase input Do(N+1) is input to delay circuit).

Allowable Subject Matter

3. Claims 4, 5, 7, 10, 20-24, 26, and 29 - 35 are allowed.

4. The following is a statement of reasons for the indication of allowable subject matter: the prior art does not teach a circuit comprising a digital filter, coefficient multiplier circuitry adapted to multiply the signal values by filter coefficients, and a summer connected to the coefficient multiplier circuitry to produce and output value wherein the summing circuitry is connected to the input lines of the signal values at different time indexes and to an adjustment input and the output of the summing circuitry is sent to a coefficient multiplying circuitry.

Response to Arguments

Applicant argues that Kobayashi does not disclose nor teach the limitation "adding the adjustment signal to the input signal" since in Kobayashi fig 5. no adjustment is added to the signal Do(N+1).

The Examiner respectfully disagrees. Kobayashi discloses broad claim 13. From figure 5, K2 x Do(N+1) added two K1 x Don meets the claimed "adding the adjustment signal to the input signal". Claim 13 simply recites adding and unfiltered offset to the output and adding the adjustment signal to the input signal. The Examiner maintains that Kobayashi meets the claimed

limitation. The Examiner urges Applicants to expand on the claimed "adding" step to overcome the Kobayashi reference.

Applicant argues that the Examiner has fails to the proper rationale or evidence to show that Kobayashi inherently discloses constraining a phase signal within a finite preset range.

Please see rejection above.

Applicant argues that Jack teaches to change hue by introducing a phase offset, conversely the present application teaches to adjust phase by an integer multiple of 360 deg to avoid any change in hue. Secondly, Jack teaches to change phase to compensate for transmission problems. Conversely the present application teaches to adjust phase by an integer multiple of 360 deg to mitigate problems other than transmission problems. Thus Jack teaches away from the claimed invention.

The Examiner concurs. The claims have been allowed.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Isono et al (4,197,556) - Hue correction circuit

Sanada et al (4,091,411) - Color hue control circuit

Nakagawa et al (4,644,389) - Digital television signal processing circuit

Ekstrand (3,688,021) - Tint control

Yoshinaka et al (4,714,954) - Read start pulse generator for time base corrector

Kosaka et al (4,939,572) - Video signal processing apparatus

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 308-9051, (for formal communications intended for entry)

Or:

(703) 308- 5399 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vivek Srivastava whose telephone number is (703) 305 - 4038. The examiner can normally be reached on Monday - Thursday from 8:00 am to 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andy Faile, can be reached at (703) 305 - 4380.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist whose telephone number is (703) 305 - 3900.

VS

10/18/02

VIVEK SRIVASTAVA
PATENT EXAMINER